AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A delay analysis system for making a delay analysis of a logic circuit,

said system having a delay analysis library comprising connection information and delay time information for a plurality of circuits,

wherein, for at least one circuit of said plurality of circuits, said library further comprises logical ~~delay~~ operation information, wherein delay ~~amounts~~ time information is ~~are~~ provided for a signal ~~transmission~~ path from input terminals to output terminals of a logical circuit and wherein ~~a~~ delay ~~amount~~ time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, and wherein said delay time information for each signal path of the logical circuit of said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals corresponding to logical operation information.

2. (currently amended): A delay analysis system for making a delay analysis of a logic circuit, said system having a delay analysis library comprising connection information and delay time information for a plurality of circuits,

wherein, for each of said plurality of circuits, said library further comprises logical ~~delay~~ operation information, wherein delay ~~amounts are~~ time information is provided for a signal

~~transmission~~ path from input terminals to output terminals of a logical circuit and wherein ~~a~~ delay ~~amount~~ time information is specific to an input terminal logical state transition and resulting logical state transition at an output terminal for each circuit of said plurality of circuits, and wherein said delay time information for each signal path of said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals corresponding to logical operation information for said at least one circuit.

3. (currently amended): A method for making a delay analysis of a logic circuit, comprising ~~the steps of~~:

referencing a delay analysis library for a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation delay information, wherein delay ~~amounts~~ time information ~~are~~ is provided for a signal ~~transmission~~ path from input terminals of a logical circuit and wherein ~~a~~ delay ~~amount~~ time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of said plurality of circuits, said delay time information for each signal path of said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals as represented by logical operation information for said at least one circuit; and

if the logic circuit comprises said at least one circuit, selecting the delay time of each path of said at least one circuit from said delay time information, wherein if a selected output terminal transitions from a low state to a high state, said delay time is selected based on the input terminal

whose logical transition triggers said low state to high state transition of said selected output terminal according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, said delay time is selected based on the input terminal whose logical transition triggers said high state to low state transition of said selected output terminal according to the logical operation information.

4. (currently amended): A computer-readable medium having stored thereon a program comprising computer instructions that, when executed on a computer, perform a process for executing a delay analysis method for a logic circuit, said computer-readable medium causing a computer to execute said method, wherein said method comprises:

referencing a delay analysis library for a plurality of circuits, said delay analysis library comprising connection information, delay time information and logic operation delay information, wherein delay ~~amounts are~~ time information is provided for a signal ~~transmission~~ path from input terminals of a logical circuit and wherein ~~a~~ delay ~~amount~~ time information is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of said plurality of circuits, said delay time information for each signal path of said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals as represented by logical operation information for said at least one circuit;

if said logic circuit comprises said at least one circuit, selecting the delay time of each path of said at least one circuit from said delay time information, wherein if a selected output

terminal transitions from a low state to a high state, said delay time is selected based on the input terminal whose logical transition triggers said low state to high state transition of said selected output terminal according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, said delay time is selected based on the input terminal whose logical transition triggers said high state to low state transition of said selected output terminal according to the logical operation information; and

performing a delay calculation to determine a propagation delay time using said selected delay time of said at least one circuit.